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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)
	10/051,980	KUMAMOTO ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 April 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5,7-13 and 15-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5, 7-13 and 15-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Und r 37 CFR 1.114

1. The present Office Action is responsive to Applicant's Request for Continued Examination (RCE) filed April 22, 2004 (Certificate of Mailing date: April 19, 2004). The Examiner acknowledges the amendments to Claims 1, 2, 5, 10 and 15, and the cancellation of Claims 6 and 14. Accordingly, Claims 1-5, 7-13 and 15-22 remain pending in the instant RCE Application.

Claim Objections

2. Claim 18 is objected to because of the following informalities:

In Claim 18, line 2: "filer" should be changed to --filler--.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Kaminaga et al. (US 6,321,734 B1)*

Chia et al. (US 6,081,997)*

Baba et al. (US 6,071,755)*

Tsukagoshi et al. (US 5,804,882)*

Lin (US 6,413,801 B1)

Odashima et al. (US 5,998,243)*

Ohmori et al. (US 5,780,933)

*Previously made of record in the instant Application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 2, 3, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al.

A) As to Claims 1 and 7:

I. Lin discloses, in Fig. 4: a chip 10 comprising a top surface (i.e., the active, solder-bumped surface), a bottom surface and one or more side surfaces disposed between the top and bottom surfaces; a substrate 20 comprising an upper surface (col.3: 36-38); a plurality of reflowed solder bumps 12 (col.1: 32-36) electrically coupling the top (i.e., active) surface of chip 10 with an adjacent portion of the upper surface of substrate 20; and a monolithic element comprising solidified (cured) molding material

resulting from a single molding process (the monolithic solidified molding material element defined by the runner 42, gate 44 and cavity 46 of the molding die; see Fig. 4 and col.3: 36-col.4: 5), the monolithic element encapsulating and adhesively bonded to (i) substantially all of the one or more side surfaces (Fig. 4 and col.3: 36-39 and 66-67), (ii) a substantial portion of the upper surface, and (iii) the plurality of reflowed solder bumps 12 located in a gap between the top surface of chip 10 and the upper surface of substrate 20 (Fig. 4 and col.1: 32-36), the monolithic element including a removable portion on the upper surface of substrate 20 resulting from a runner 42 used to inject the molding material in the single molding process (col.3: 64-col.4: 5).

II. Lin discloses all the limitations of base Claim 1 and further discloses a cured liquefied molding material as the solidified molding material encapsulant of the flip chip package (Fig. 4; col.3: 64-col.4: 14) but does not identify the type of molding material.

III. Odashima et al. discloses a cured liquefied molding material as the solidified encapsulant of the flip chip package and further discloses that the molding material is the commonly used epoxy resin (col.5: 23-24; col.6: 45-49).

IV. Since Lin and Odashima et al. both teach similar fabrication of a flip chip package comprising the use of a liquefied molding material injected into mold die cavities to encapsulate a chip package and subsequently solidified (cured), then the use of an epoxy resin molding material to accomplish the encapsulation of the flip chip package, as taught by Odashima et al., would have been readily recognized in the pertinent art of Lin as a common and reliable off-the-shelf chip package encapsulant, as taught by Odashima et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in Lin, an epoxy resin molding material, in order to reliably encapsulate the flip chip package, as taught by Odashima et al.

B) As to Claim 2:

I. Lin discloses all the limitations of base Claim 1 including chip 10 having a bottom surface, i.e., the non-active back surface of the chip (Fig. 4), but does not disclose that the solidified resin does not encapsulate the bottom surface of the chip; rather, Lin discloses that the entire chip, including the bottom surface is encapsulated by the resin (Fig. 4; col.3: 64-67).

II. Odashima et al. discloses a fabrication of a flip chip package, similar to that of Lin, wherein the solidified resin encapsulates the entire chip 12 (Figs. 2A,B,C and 3). However, Odashima et al. further discloses another embodiment wherein the mold structure is modified such that the bottom surface (i.e., non-active back surface) of the chip 12 is not covered by the solidified resin; i.e., the bottom surface of chip 12 (referenced as “the top of the semiconductor chip 12” in Odashima et al.) is exposed to the ambient environment (Figs. 10A,B and 4B) in order to make the package even thinner (col.10: 33-37).

III. Since both Lin and Odashima et al. are both in the art of fabricating flip chip packages of minimal size to meet consumer-driven industrial miniaturization requirements, then the modification of the molding die, as taught by Odashima et al., to produce a packaged flip chip having the bottom, non-active, back surface of the chip

exposed (i.e., not covered by the solidified resin) in order to produce a thinner (i.e., low profile) flip chip package would have been readily recognized in the pertinent art of Lin.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the height of the molding die of Lin such that the resin encapsulant does not cover the bottom (non-active) surface of the chip, thus leaving the bottom chip surface of the chip exposed (i.e., not encapsulated by the solidified resin) and thereby forming, in Lin, a flip chip package that has a thinner profile to meet the miniaturization and chip scale package requirements of an application, as taught by Odashima et al.

C) As to Claim 3, modified Lin discloses that the resin further comprises a filler material (col.2: 8-12).

D) As to Claim 5, the resin encapsulates substantially all of the one or more side surfaces of chip 10 (Fig. 4 and col.3: 36-39 and 66-67).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al., as applied to Claim 3, above, and further in view of Chia et al. and Kaminaga et al.

I. Lin, as modified by Odashima et al., discloses all the limitations of base Claim 1 and further discloses that the cured liquefied molding material, comprising particulate filler material, is the solidified epoxy resin encapsulant of the flip chip package (Fig. 4; col.2: 8-12; col.3: 43-49; col.3: 64-col.4: 14), the encapsulant with filler performing the function of covering the chip (col.3: 64-67) so as to protect the chip against ambient contaminants, and also serving as an underfill that provides stress relief in the reflowed

solder bumps due to coefficients of thermal expansion (CTE) mismatch between chip 10 and substrate 20 during package operation (col.1: 25-35). Lin, as modified by Odashima et al., does not identify the type of filler.

II. Chia et al., in the same packaging art as Lin, discloses silica particles in a solidified epoxy resin encapsulant 32 that are electrically insulating, thermally conductive and also exhibit the property of having substantially the same CTE as that of the solder bumps, thereby further enhancing stress relief in the reflowed solder bumps during package operation (Fig. 3; col.6: 40-51). Chia et al. is silent as to the shape and size of the silica particles.

III. Kaminaga et al., in the same packaging art as Lin and Chia et al., teaches an epoxy resin encapsulant comprising a filler material of silica spherical particles, said encapsulant with filler not only reduces the TCE of epoxy resin encapsulant 4 to substantially the same CTE as that of the solder bumps (as in Chia et al.) but also prevents discrete packaging parts and the substrate from being damaged, said damage caused by the sharp edges of non-spherical filler particles used in prior art packages, and furthermore teaches that it is preferable that the spherical particles be very small, i.e., "microspheres" in order to enhance the fluidity of the resin encapsulant, thereby ensuring that the resin completely encapsulates the chip and its bumps in the transfer mold (Fig. 3; col.5: 48-51; col.7: 3-28 and 61-65; col.10: 55-col.11: 3).

IV. Since Lin as modified by Odashima et al., Chia et al. and Kaminaga et al. are all in the same packaging art that includes encapsulation of a chip mounted on a substrate, and are solving similar TCE mismatch problems and heat dissipation

problems, then the use of silica particles (Chia et al.) that are very small spheres, i.e., microspheres (Kaminaga et al.) would have been readily recognized for all the above-cited benefits taught by Chia et al. and Kaminaga et al., respectively, in the pertinent packaging art of modified Lin wherein the CSP is encapsulated with a molding material.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the epoxy resin molding material of modified Lin with the epoxy resin molding material comprising silica microspheres, as taught by Chia et al. and Kaminaga et al., in order to: (i) enhance solder bump stress relief and (ii) prevent discrete packaging parts and the substrate from being damaged, in the CSP of modified Lin, said damage caused by the sharp edges of non-spherical filler particles used in prior art packages, and furthermore, (iii) by virtue of the small particle size (microspheres) taught by Kaminaga et al., ensure that the molding resin material completely encapsulates the chip and its bumps in the molding process of modified Lin.

8. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al., as applied to Claim 1, above, and further in view of Ohmori et al.

A) As to Claims 8 and 10:

I. Lin, as modified by Odashima et al., discloses all the limitations of base Claim 1 and further discloses that substrate 20 is part of a chip scale package (CSP) which is an effective packaging structure for use in meeting the consumer demand for miniaturization of electronic products (col.1: 11-24).

II. Modified Lin further teaches that a CSP is only 20% larger than the bare die itself but does not specify the dimensions of the substrate 20; in particular, does not specify that the substrate 20 has a small thickness (i.e., that the substrate 20 is thin) and/or its exact thickness measurement.

III. Ohmori et al. discloses fabricating a semiconductor package (including flip chip packages; col.6: 25-31; col.8: 5-7) including a substrate 11 in Fig. 1 (substrate 18 in Figs. 2-4) that is part of a CSP for use in meeting the consumer demand for miniaturization of electronic products and further teaches that, in order to fabricate a CSP package, the substrate is thin (col.1: 8-24; col.5: 36-38). In particular, Ohmori et al. teaches that the substrate has a thickness in a range between 0.05mm and 0.5mm; specifically, a thickness between 0.2mm and 0.3mm (col.5: 19-21).

IV. Since modified Lin and Ohmori et al. are both similarly fabricating CSP packages for use in meeting the demand for miniaturization of electronic products, then the small thickness dimension (i.e., "thinness") of the CSP substrate specified by Ohmori et al. would have been readily recognized as effective for the substrate of the same type of CSP package in the pertinent art of modified Lin.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in the CSP of modified Lin, a thin substrate having a thickness dimension between 0.05mm and 0.5mm, as taught in the CSP of Ohmori et al., in order to fabricate CSP devices that meet the demand for miniaturization of the electronic products in which they are applied.

B) As to Claim 9:

I. Lin, as modified by Odashima et al., discloses all the limitations of base Claim 1 but is silent as to the material composition of chip scale package substrate 20.

II. Ohmori et al. discloses fabricating a semiconductor package (including flip chip packages; col.6: 27-31; col.8: 5-7) including a substrate 11 in Fig. 1 (substrate 18 in Figs. 2-4) comprised of a polymeric material (col.5: 37-39; col.6: 17-20) in order to form a thin substrate that meets the all chip scale package (CSP) dimensions required for small and compact devices that are consumer-demanded in the electronics industry (col.1: 17-24).

III. Since modified Lin (col.1: 11-24) and Ohmori et al. are in the same art of fabricating CSP packages that meet the dimensional requirements that enable the manufacture of smaller consumer electronic devices, the use of polymeric materials for forming such a small and thin package substrate for a CSP, as taught by Ohmori et al., would have been readily recognized in the pertinent CSP fabrication art of modified Lin.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in forming the CSP substrate of modified Lin, any of the polymeric materials taught by Ohmori et al. for making a CSP substrate having dimensions that form a thin and small CSP for use in manufacturing miniaturized consumer electronics desired in the electronics industry.

9. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al., as applied to Claim 1, above, and further in view of Baba et al.

A) As to Claim 11:

I. Modified Lin discloses all the limitations of base Claim 1 including a chip 10 electrically coupled with substrate 20 (Fig. 4) but does not teach at least one passive component electrically coupled with substrate 20.

II. Baba et al. discloses, in Fig. 20, a passive component 53, which may be a chip capacitor or a chip resistor, coupled to substrate 34 along with chips 31 (col.12: 31-35), typically functioning as a noise decoupling capacitor for suppressing noise on the power line and preventing such noise spikes from reaching the power contacts of chip 31, or current or impedance control (resistor), for ensuring proper performance of the device package.

III. Since modified Lin teaches encapsulating a device package formed of chip 10 and package substrate 20, and since the problem of power line noise, current or impedance control, as solved by the passive device in Baba et al., would have been readily recognized in the pertinent art of modified Lin for the same functions, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify modified Lin by including on the device package substrate of modified Lin a passive device (capacitor or resistor), as taught in Baba et al., in order to provide a noise decoupling capacitor, or, current or impedance controlling resistor in the CSP of modified Lin, as taught in Baba et al., thereby improving the performance of the device package of modified Lin.

B) As to Claim 12, it is apparent that, as an inherent result of the encapsulation process disclosed in Fig. 4 of modified Lin, the solidified resin molding material in the device package fabrication taught by Lin (see Fig. 4), as modified by Odashima et al.

and Baba et al., fills a gap between a first surface (i.e., the lower non-contact surface) of the passive component, elevated above the substrate by the conductive joining material, and an adjacent surface of the substrate (as taught in modifier reference Baba et al., Fig. 20: see passive component 53 mounted on the surface of substrate 34, elevated by the conductive joining material and encapsulated, along with the chips 31, in the manner taught by Lin in Fig. 4), just as the solidified resin is disclosed to fill the gap between the top (active and bumped) surface of chip 10 and the upper surface of substrate 20 in said encapsulation process disclosed in Fig. 4 of modified Lin. [Examiner's Remark: *the Examiner notes that the Applicant's disclosure--see Fig. 2F and lines 3-7 of paragraph [0007] in the Specification--teaches the same type of chip resistors and chip capacitors as the chip resistor or capacitor 53 taught by Baba et al. in Fig. 20 and col.12: 34-35*].

C) As to Claim 13, it is apparent that, as an inherent result of the encapsulation process disclosed in Fig. 4 of modified Lin, the solidified resin of said encapsulation process fully encapsulates the passive component (as in Fig. 20, element 53, of modifier reference Baba et al.), just as the solidified resin is disclosed to fully encapsulate chip 10 in said encapsulation of process of modified Lin.

10. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al.

A) As to Claim 15:

I. Lin discloses, in Fig. 4: a substrate 20 comprising a first (upper) surface (col.3: 36-38); a chip 10 comprising a first surface (i.e., the active, solder-bumped surface), a

second surface and one or more edges, the first surface of chip 10 being coupled with the first surface of substrate 20 by a plurality of solder bumps 12 (col.1: 32-36), the solder bumps 12 electrically providing electrical connection between chip 10 and substrate 20; and a solid (cured) molding material element (the solid molding material element defined by the runner 42, gate 44 and cavity 46 of the molding die; see Fig. 4 and col.3: 36-col.4: 5) resulting from a process of injecting liquid molding material into a mold containing chip 10 and substrate 20 in a single molding process (col.3: 43-49), the solid molding material element encapsulating and bonding to the first surface of chip 10, the one or more edges of chip 10 (Fig. 4 and col.3: 36-39 and 66-67), and the plurality of solder bumps 12 (Fig. 4)(ii) a substantial portion of the upper surface, and (iii) the plurality of solder bumps 12 (Fig. 4 and col.1: 32-36), the solid molding material element including a removable portion on the first surface of substrate 20 resulting from injection of the molding material through a runner 42 during the molding process (col.3: 64-col.4: 5).

II. Lin discloses all the limitations of base Claim 1 and further discloses a cured liquefied molding material as the solidified molding material encapsulant of the flip chip package (Fig. 4; col.3: 64-col.4: 14) but does not identify the type of molding material.

III. Odashima et al. discloses a cured liquefied molding material as the solidified encapsulant of the flip chip package and further discloses that the molding material is the commonly used epoxy resin (col.5: 23-24; col.6: 45-49).

IV. Since Lin and Odashima et al. both teach similar fabrication of a flip chip package comprising the use of liquefied molding material injected into mold die cavities

to encapsulate a chip package and subsequently solidified (cured), then the use of an epoxy resin molding material to accomplish the encapsulation of the flip chip package, as taught by Odashima et al., would have been readily recognized in the pertinent art of Lin as a common and reliable off-the-shelf chip package encapsulant, as taught by Odashima et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in Lin, an epoxy resin molding material, in order to reliably encapsulate the flip chip package, as taught by Odashima et al.

B) As to Claim 16:

I. Lin discloses all the limitations of base Claim 15 including chip 10 having a second surface, i.e., the non-active back surface of the chip (Fig. 4), but does not disclose that the solidified resin is not bonded with the second surface of the chip; rather, Lin discloses that the entire chip, including the second surface is encapsulated by the resin (Fig. 4; col.3: 64-67).

II. Odashima et al. discloses a fabrication of a flip chip package, similar to that of Lin, wherein the solidified resin encapsulates the entire chip 12 (Figs. 2A,B,C and 3). However, Odashima et al. further discloses another embodiment wherein the mold structure is modified such that the solid resin is not bonded with the second surface (i.e., non-active back surface) of the chip 12; i.e., the second surface of chip 12 (referenced as “the top of the semiconductor chip 12” in Odashima et al.) is exposed to the ambient environment (Figs. 10A,B and 4B) in order to make the package even thinner (col.10: 33-37).

III. Since both Lin and Odashima et al. are both in the art of fabricating flip chip packages of minimal size to meet consumer-driven industrial miniaturization requirements, then the modification of the molding die, as taught by Odashima et al., to produce a packaged flip chip such that the solid resin is not bonded with a second (non-active) surface of the chip (i.e., the second surface of the chip is exposed) in order to produce a thinner (i.e., low profile) flip chip package would have been readily recognized in the pertinent art of Lin.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the height of the molding die of Lin such that the solid resin encapsulant does is not bonded with the second (non-active) surface of the chip, thus leaving the second surface of the chip exposed and thereby forming, in Lin, a flip chip package that has a thinner profile to meet the miniaturization and chip scale package requirements of an application, as taught by Odashima et al.

C) As to Claim 17:

Lin, as modified by Odashima et al., discloses all the limitations of Claim 16, and further discloses that the process of Odashima et al. (Figs. 10A,B and 4B) which modified the device of Lin, in accordance with the requirement of Claim 16, includes the intermediate fabrication step structure wherein the second (non-active, non-encapsulated) surface of chip 12 was in contact with the mold during the process of injecting liquid resin into the mold (Figs. 10A,B; col.11: 28-32).

D) As to Claim 18, modified Lin further discloses that the resin further comprises a filler material (col.2: 8-12).

11. Claims 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al., as applied to Claim 18, above, and further in view of Chia et al. and Kaminaga et al.

As to Claims 19, 20 and 22:

I. Lin, as modified by Odashima et al., discloses all the limitations of base Claim 15 and further discloses that the cured liquefied molding material, comprising particulate filler material, is the solidified epoxy resin encapsulant of the flip chip package (Fig. 4; col.2: 8-12; col.3: 43-49; col.3: 64-col.4: 14), the epoxy encapsulant with filler performing the function of covering the chip (col.3: 64-67) so as to protect the chip against ambient contaminants, and also serving as an underfill that provides stress relief in the reflowed solder bumps due to coefficients of thermal expansion (CTE) mismatch between chip 10 and substrate 20 during package operation (col.1: 25-35). Lin, as modified by Odashima et al., does not identify the type of filler particles used in the epoxy resin.

II. Chia et al., in the same packaging art as Lin, discloses silica particles in a solidified epoxy resin encapsulant 32 that are electrically insulating, thermally conductive and also exhibit the property of having substantially the same CTE as that of the solder bumps, thereby further enhancing stress relief in the reflowed solder bumps during package operation (Fig. 3; col.6: 40-51). Chia et al. is silent as to the shape and size of the silica particles.

III. Kaminaga et al., in the same packaging art as Lin and Chia et al., teaches an epoxy resin encapsulant comprising a filler material of silica spherical particles, said

encapsulant with filler not only reduces the TCE of epoxy resin encapsulant 4 to substantially the same CTE as that of the solder bumps (as in Chia et al.) but also prevents discrete packaging parts and the substrate from being damaged, said damage caused by the sharp edges of non-spherical filler particles used in prior art packages, and furthermore teaches that it is preferable that the spherical particles be very small, i.e., "microspheres" in order to enhance the fluidity of the resin encapsulant, thereby ensuring that the resin completely encapsulates the chip and its bumps in the transfer mold (Fig. 3; col.5: 48-51; col.7: 3-28 and 61-65; col.10: 55-col.11: 3).

IV. Since Lin as modified by Odashima et al., Chia et al. and Kaminaga et al. are all in the same packaging art that includes encapsulation of a chip mounted on a substrate, and are solving similar TCE mismatch problems and heat dissipation problems, then the use of silica particles (Chia et al.) that are very small spheres, i.e., microspheres (Kaminaga et al.) would have been readily recognized for all the above-cited benefits taught by Chia et al. and Kaminaga et al., respectively, in the pertinent packaging art of modified Lin wherein the CSP is encapsulated with a molding material.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the epoxy resin molding material of modified Lin with the epoxy resin molding material comprising silica microspheres, as taught by Chia et al. and Kaminaga et al., in order to: (i) enhance solder bump stress relief and (ii) prevent discrete packaging parts and the substrate from being damaged, in the CSP of modified Lin, said damage caused by the sharp edges of non-spherical filler particles used in prior art packages, and furthermore, (iii) by virtue of the small

particle size (microspheres) taught by Kaminaga et al., ensure that the molding resin material completely encapsulates the chip and its bumps in the molding process of modified Lin.

12. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Odashima et al., Chia et al. and Kaminaga et al., as applied to Claim 19, above, and further in view of Tsukagoshi et al.

I. Lin, as modified by Odashima et al., and further modified by Chia et al. and Kaminaga et al., teaches microspheres comprised of silica (see col.5: 48-51, col.7: 3-28 and 61-65, and col.10: 66-col.11: 3 of Kaminaga et al.) but does not teach microspheres comprised of glass.

II. Tsukagoshi et al. discloses an epoxy resin underfill 11 (col.7: 16-26) used to bond chip 1 to substrate 4, the epoxy resin 11 comprising micron-sized insulating filler particles (col.7: 53-62 and col.8: 42-48), wherein these micron-sized insulating filler particles can be spherical and made of silica or glass, among other materials which are recognized equivalents for performing the functions of fillers in epoxy resin underfills (col.8: 49-55).

III. Since Tsukagoshi et al., and Lin as modified by Chia et al. and Kaminaga et al., are in the same art of assembling electronic packages using epoxy resin underfills with microspherical silica fillers, the use of the equivalent microspherical glass fillers taught by Tsukagoshi et al. would have been readily recognized in the pertinent art of modified Lin to perform the same functions of the microspherical silica fillers in the epoxy resin molding material of modified Lin.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the microspherical silica fillers of modified Lin with the equivalent microspherical glass fillers, as taught in Tsukagoshi et al., for the purpose of controlling package reliability factors, such as the resin viscosity and/or the thermal expansion mismatch problems between the packaging elements, recognized and solved by the use of the equivalent microspherical silica fillers in modified Lin, said replacement of silica microspherical fillers with glass microspherical fillers (taught as equivalents by Tsukagoshi et al.) being influenced by matters of cost and package reliability relating to the types of materials being used in the various elements of the package (e.g., substrate materials, composition of solder balls, etc.) of modified Lin, in which the epoxy resin with the microspherical fillers is being used as the molding material.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references teach a solid resin encapsulant including a removable portion on the surface of the substrate resulting from injection of the resin through a runner during the molding process, including applicability of the disclosed molding process to flip chip packages, as well as wire bond packages:

Haji (US 6,432,751 B1): Figs. 9 and 10.

Huang et al. (US 6,083,775): Figs. 3, 4 and 5.

Wensel (US 5,969,427): Figs. 5-9.

Woosely et al. (US 5,656,549): Fig. 2; col.4: 37-50.

Freyman et al. (US 5,635,671): Fig. 8A and 8B.

Juskey et al. (US 5,542,171): Figs. 1 and 2.

b) Ueda et al. (US 5,196,917) discloses an encapsulation of a chip on a carrier tape including the removal of a portion of the encapsulant resulting from injection of the resin 11 through a gate 17 of mold 10 and an opening 15 in a portion of the film 1 (Figs. 2 and 3; col.4: 63-col.5: 3).

c) Chiu et al. (US 6,498,054 B1) discloses passive devices 301 and a chip 10 mounted on a substrate 30 and further discloses an underfill process and apparatus that enables an underfilling of flip chip 10 that is unobstructed by passive devices 301 (col.2: 31-34; col.4: 38-43).

d) Lee et al. (US 5,620,928) discloses an ultra-thin BGA package wherein a chip 40 may be electrically connected to the substrate 84 by flip-chip bonding or wire bonding. After the chip bonding process is complete, the finished package is removed from support substrate 38 (Figs. 4A and 4B; col.6: 42-53).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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